AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/027,353
Filed: December 19, 2001
Inventors:
Walter T. Nixon
Fay Chong, Jr.

Title: Cache Accumulator Memory with an Associativity Mechanism

Examiner: Tsai, Sheng Jen
Group/Art Unit: 2186
Atty. Dkt. No: 5681-05300

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Robert C. Kowert
Name of Registered Representative

Signature

December 1, 2005
Date

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants request review of the rejection of claims 1-36 in the Office Action of October 13, 2005 in the above-identified application. The instant Office Action reopens prosecution following Applicants' Appeal Brief mailed August 29, 2005. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reasons stated below.

Claims 1-36 remain pending in the application. Reconsideration of the present case is earnestly requested in light of the following remarks. Please note that for brevity, only the primary arguments directed to the independent claims and selected dependent claims are presented, and that additional arguments, e.g., directed to the subject matter of the remaining dependent claims, will be presented if and when the case proceeds to Appeal.

Claims 1-3, 5, 6, 9, 10, 13-23, 26 and 28-36 are rejected under 35 U.S.C. § 102(b) as being anticipated by Crater et al. (U.S. Patent 5,146,588) (hereinafter "Crater"). Various dependent claims are rejected under 35 U.S.C. § 103(a) as indicated in the Office Action. The following clear errors in the Examiner's rejection are noted.

Crater fails to teach or suggest all of the limitations of Applicants' claim 1. Specifically, Crater fails to teach or suggest an apparatus including a cache accumulator memory coupled to a memory and a functional unit, wherein the cache accumulator memory comprises a plurality of block storage locations, wherein the cache accumulator memory is configured to receive a set of one or more instructions to perform a first accumulation operation, wherein the cache accumulator memory is configured as a cache of the memory, and wherein the cache accumulator memory is configured to accumulate an intermediate result of the first accumulation operation, wherein the intermediate result is both a result of and an operand of the first accumulation operation.

In rejecting claim 1, the Examiner asserts that the redundancy accumulator 301 of Crater corresponds to Applicant's claimed cache accumulator memory, and that Crater's inclusion of redundancy accumulator 301 within a unit denoted as "cache 113" is a disclosure of Applicant's recitation that the cache accumulator memory is a cache of a memory. However, the Examiner's assertion is not supported by the structure disclosed by Crater. Although Crater discloses cache 113, Crater does not describe in any way that redundancy accumulator 301 is itself configured as a cache of any memory. Crater describes the function of redundancy accumulator 301 as simply to temporarily "...store the intermediate result of ... redundancy calculations until all of the physical tracks have been included in the redundancy calculation." (col. 7, lines 55-57). Crater does not disclose any relationship between the contents of redundancy accumulator 301 and other data storage elements within cache 113, much less a caching relationship as recited in Applicants' claim.

The Examiner seems to imply that because Crater's redundancy accumulator 301 is included within a cache, redundancy accumulator 301 must itself function as a cache. This simply does not follow. Crater discloses that cache 113 functions as a cache with respect to data transfers between host processors 11, 12 and disk drive subsets 103 (FIG. 1 and col. 6, lines 7-12, 38-39). This operation occurs at an entirely different level of scope than the relationship between cache 113 and its component, redundancy accumulator 301. That is, the fact that cache 113 functions as a cache with respect to host processors 11, 12 and disk drive subsets 113 does not entail that redundancy accumulator 301 functions as a cache with respect to cache 113 or anything else, and in fact Crater discloses no such relationship.

Applicants note that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). For at least the reasons given above, Crater clearly fails to meet this standard with respect to claim 1. A similar argument applies to independent claims 20, 33 and 34, which recite limitations similar to those of claim 1. Applicants therefore submit that each of these claims is not anticipated by Crater.

Crater further fails to teach or suggest all of the limitations recited in Applicants' claim 5. Specifically, Crater does not teach or suggest that the cache accumulator memory is configured to load a copy of the block operand into the cache accumulator memory from the memory in response to the block operand not being present in the cache accumulator memory when the instruction is received. In rejecting claim 5, the Examiner asserts that in Crater, the first block operand is loaded into redundancy accumulator 301 from the disk drives via the DATA INPUT BUS and latch 303. However, Crater does not disclose that redundancy accumulator 301 obtains its input data from a memory of which it is configured as a cache, nor doing so in response to the block operand not being present in the accumulator. As argued above, Crater's redundancy accumulator 301 is

not configured as a cache of any sort. Crater specifically discloses that data is received into accumulator 301 not from any memory, but rather that "[i]n operation, a byte from a received physical track is read into latch 303..." (col. 8, lines 56-57). Further, Crater shows in FIG. 2 and FIG. 3 that this data bus corresponds to the DEV ADT bus, which interfaces data directly from disk drive subset 103. Thus, Crater's redundancy accumulator 301 does not operate to load data from a memory of which it is configured as a cache in response to that data not being present, as recited in claim 5. Therefore, Crater further fails to anticipate claim 5.

Numerous other ones of the dependent claims recite additional distinctions over what is disclosed in Crater or the other cited references. However, as the independent claims have been shown to be distinguishable, further discussion of the dependent claims is unnecessary at this time.

In light of the foregoing remarks, Applicants submit the application is in condition for allowance, and notice to that effect is respectfully requested. If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 501505/5681-05300/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☒ Notice of Appeal

Respectfully submitted,

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